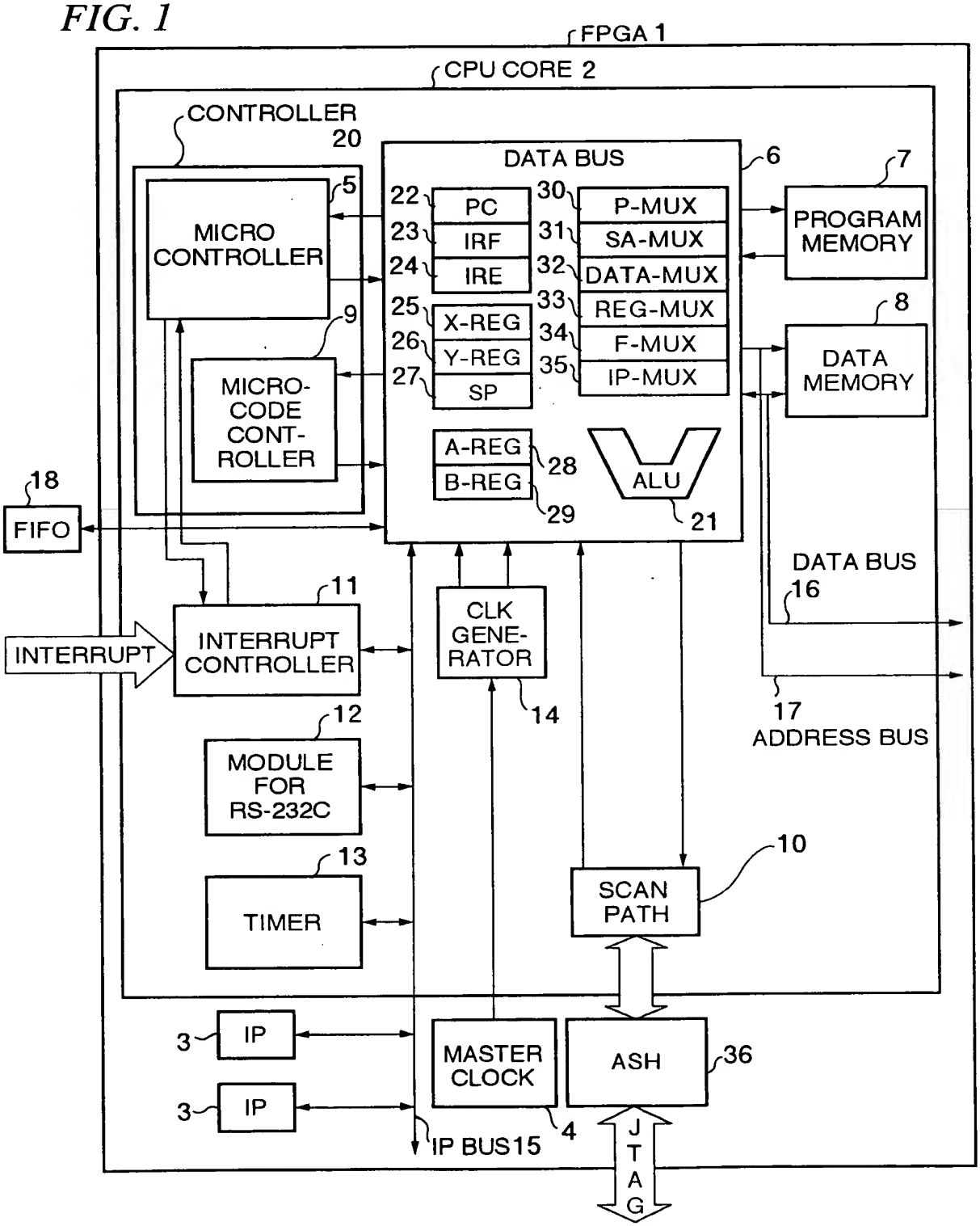
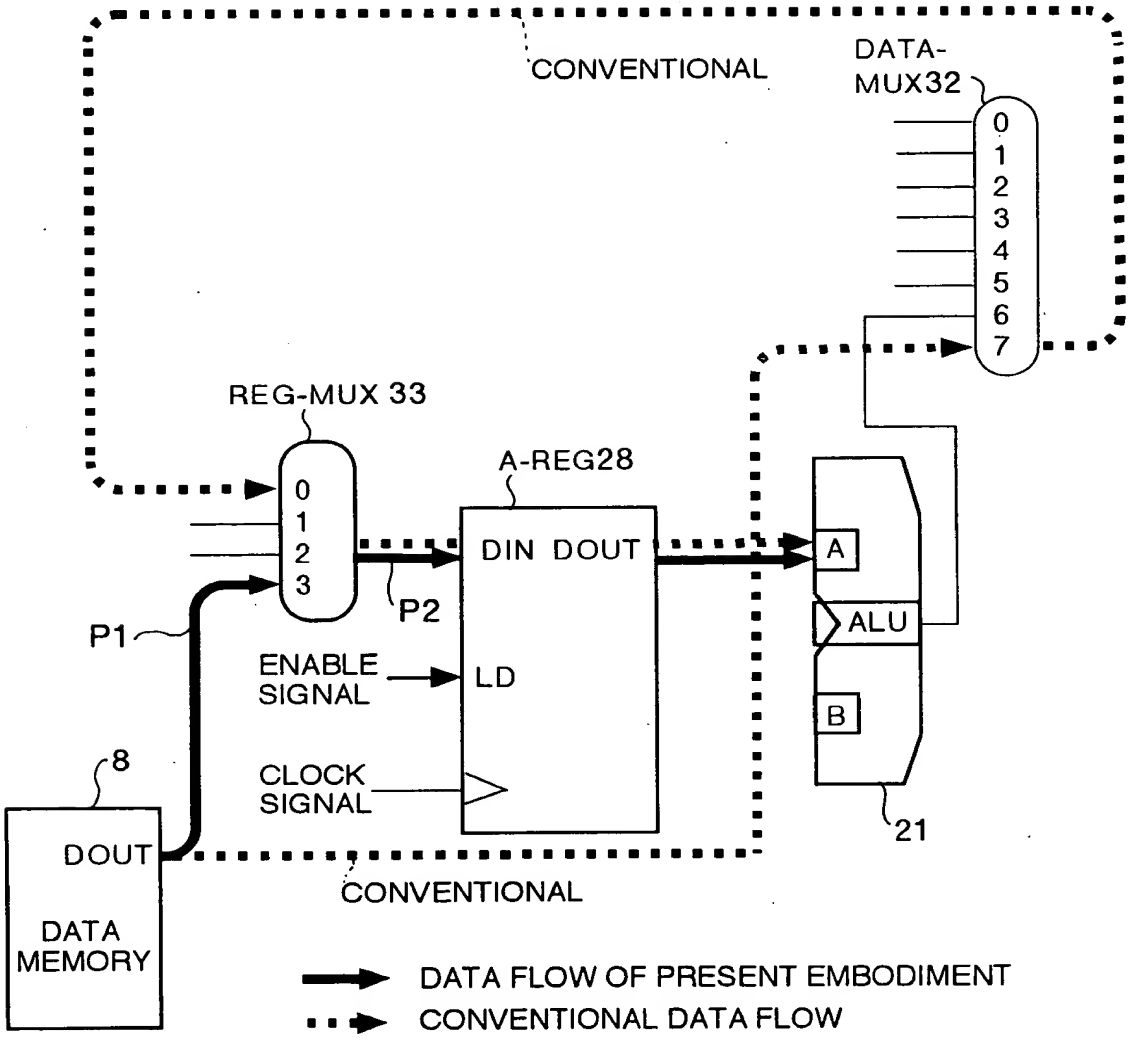
FIG. 1



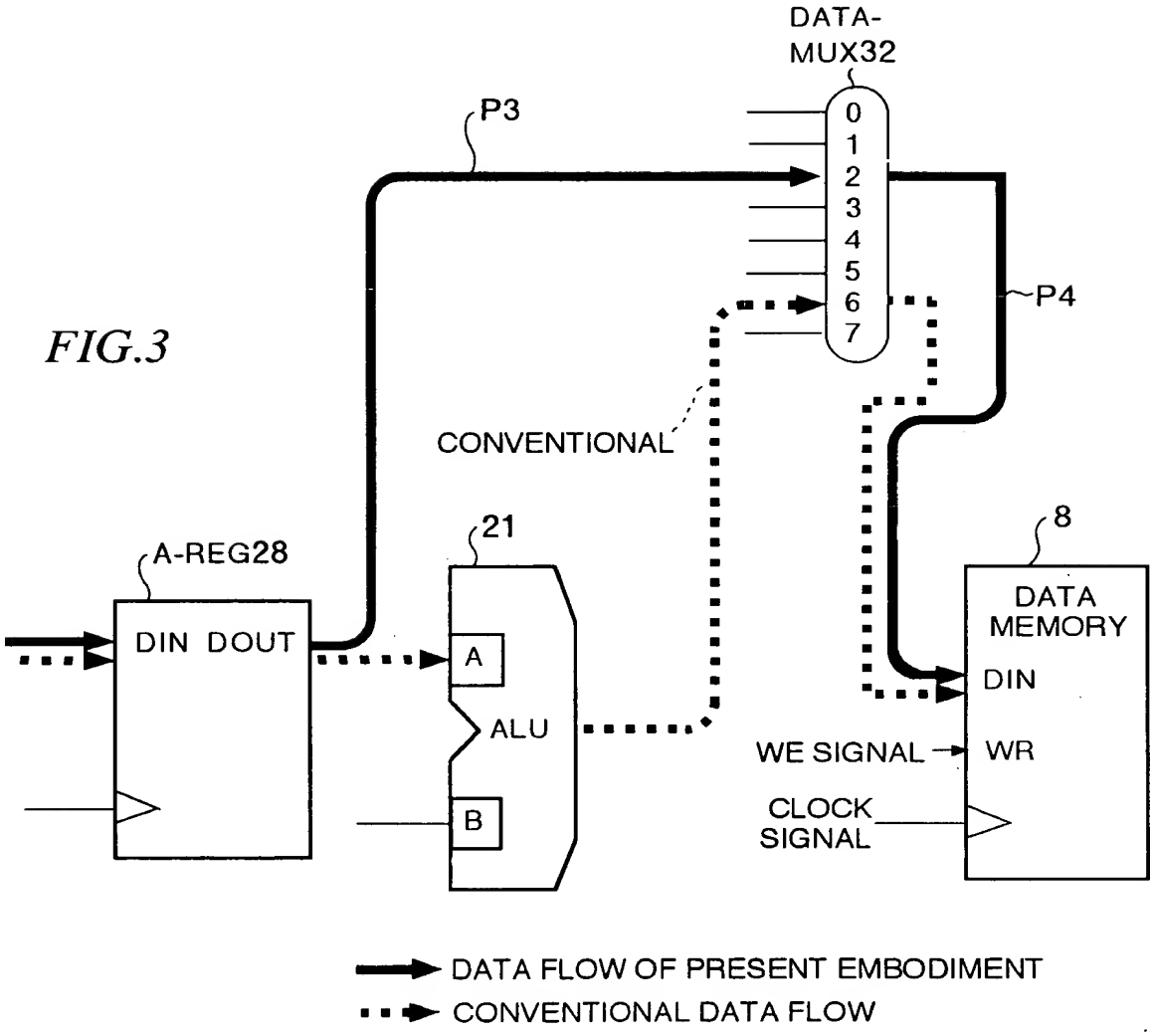
09/22/2004, 01259901

FIG.2


CONVENTIONAL
DATA-
MUX32
0
1
2
3
4
5
6
7
REG-MUX 33
0
1
2
3
A-REG28
DIN DOUT
A
ALU
B
P1
P2
ENABLE
SIGNAL
LD
CLOCK
SIGNAL
8
DOUT
DATA
MEMORY
21
CONVENTIONAL
DATA FLOW OF PRESENT EMBODIMENT
CONVENTIONAL DATA FLOW

EP0572760A2

FIG.3



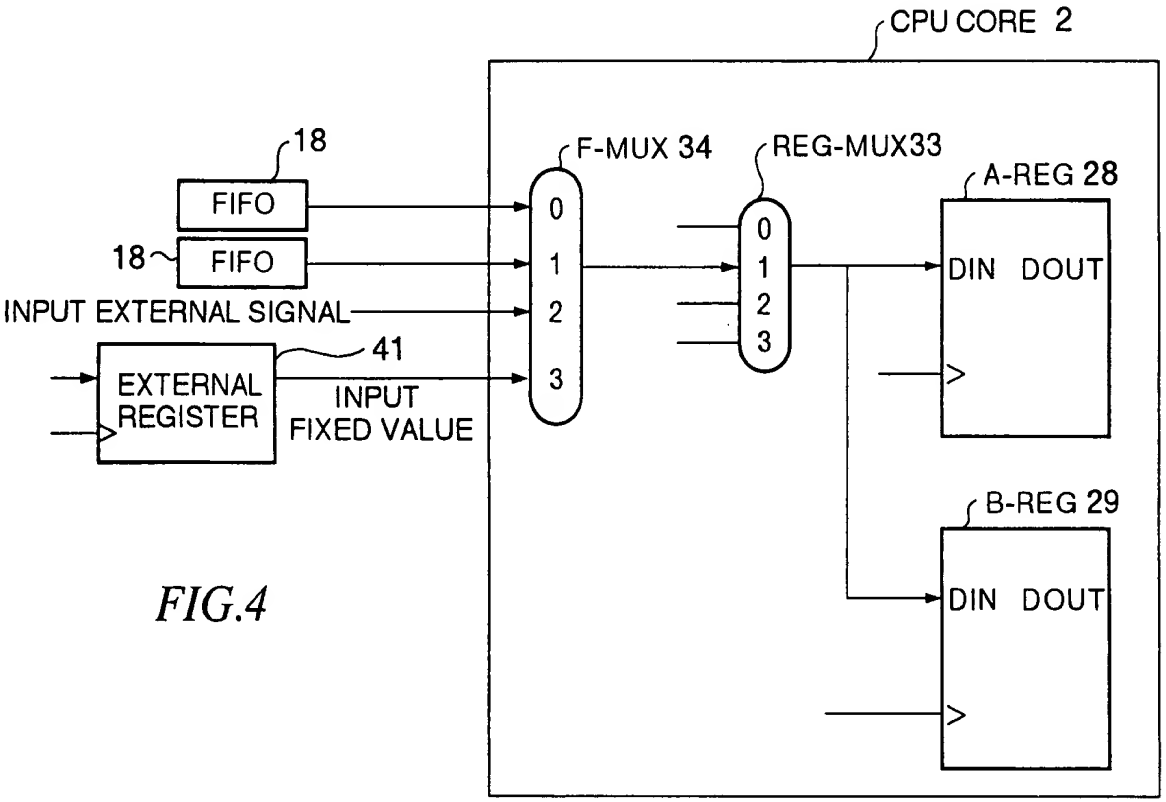
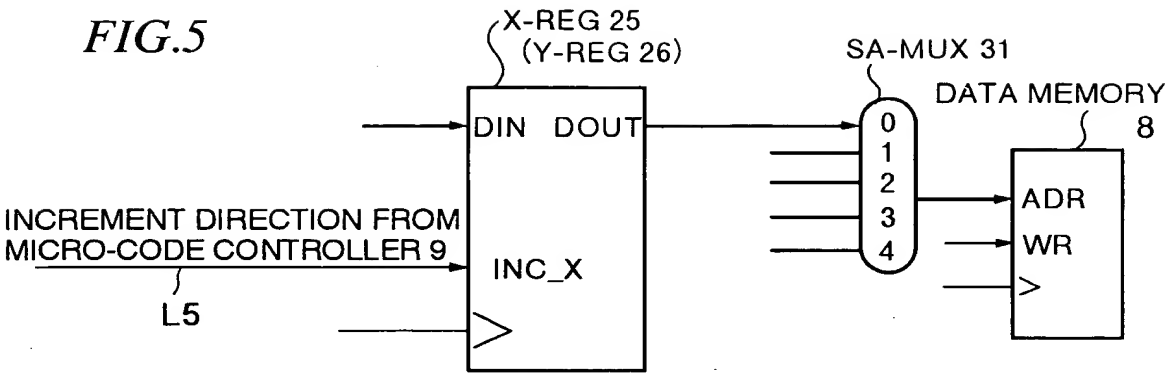

CPU CORE 2
18
FIFO
18
FIFO
INPUT EXTERNAL SIGNAL
EXTERNAL REGISTER
41
INPUT FIXED VALUE
F-MUX 34
0
1
2
3
REG-MUX33
0
1
2
3
A-REG 28
DIN DOUT
B-REG 29
DIN DOUT

FIG.4

FIG.5

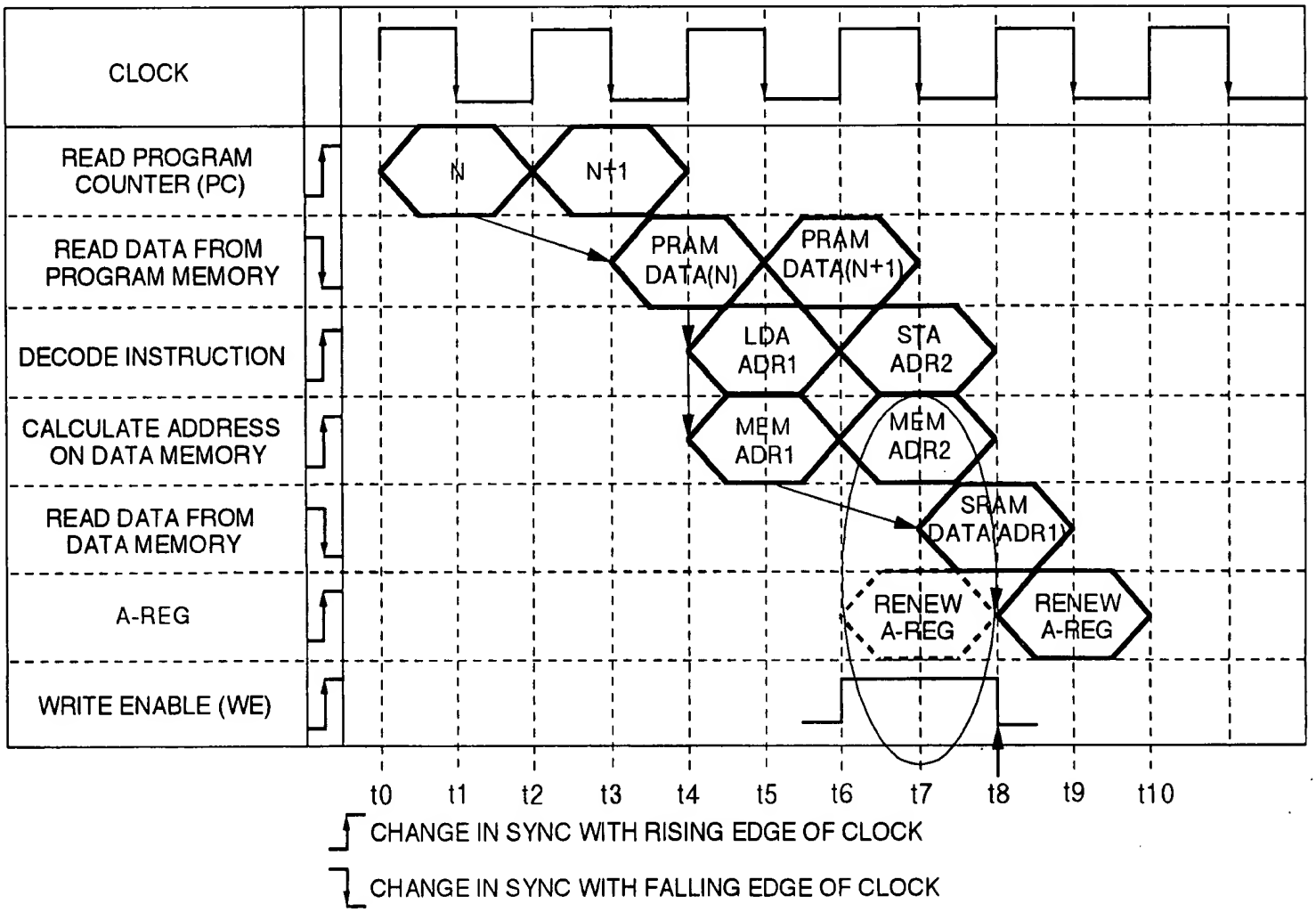


EP 0 512 420 A2

T062T0" 72027760

FIG.6 PRIOR ART

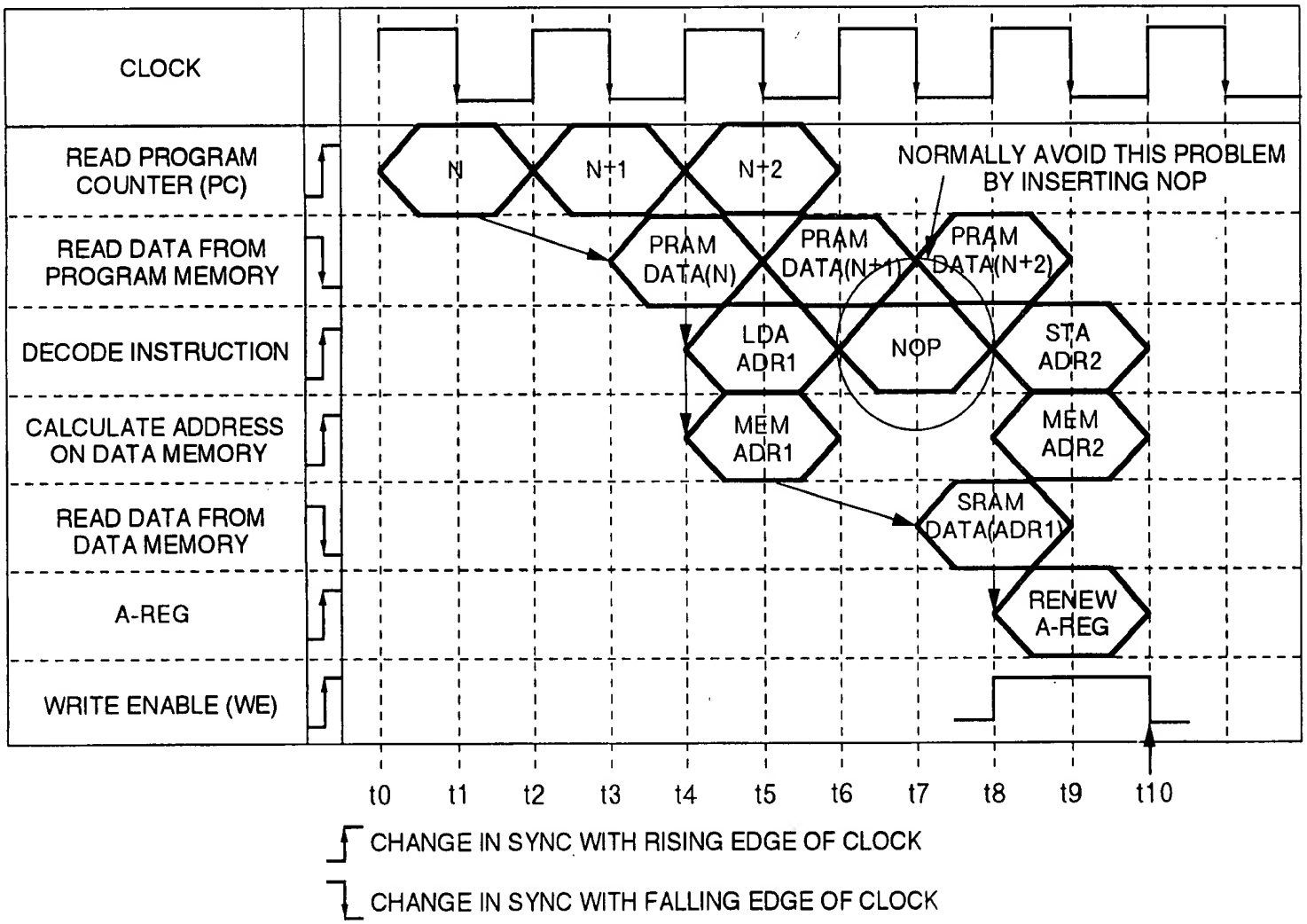
EXAMPLE OF CONTROL IN SINGLE CLOCK (IN LDA & STA CONTINUOUS COMMAND)



T062T0" 72027760

FIG.7

EXAMPLE OF SOLUTION BY INSERTING NOP



CONTROL METHOD OF CPU CORE IN PRESENT EMBOMDIMENT

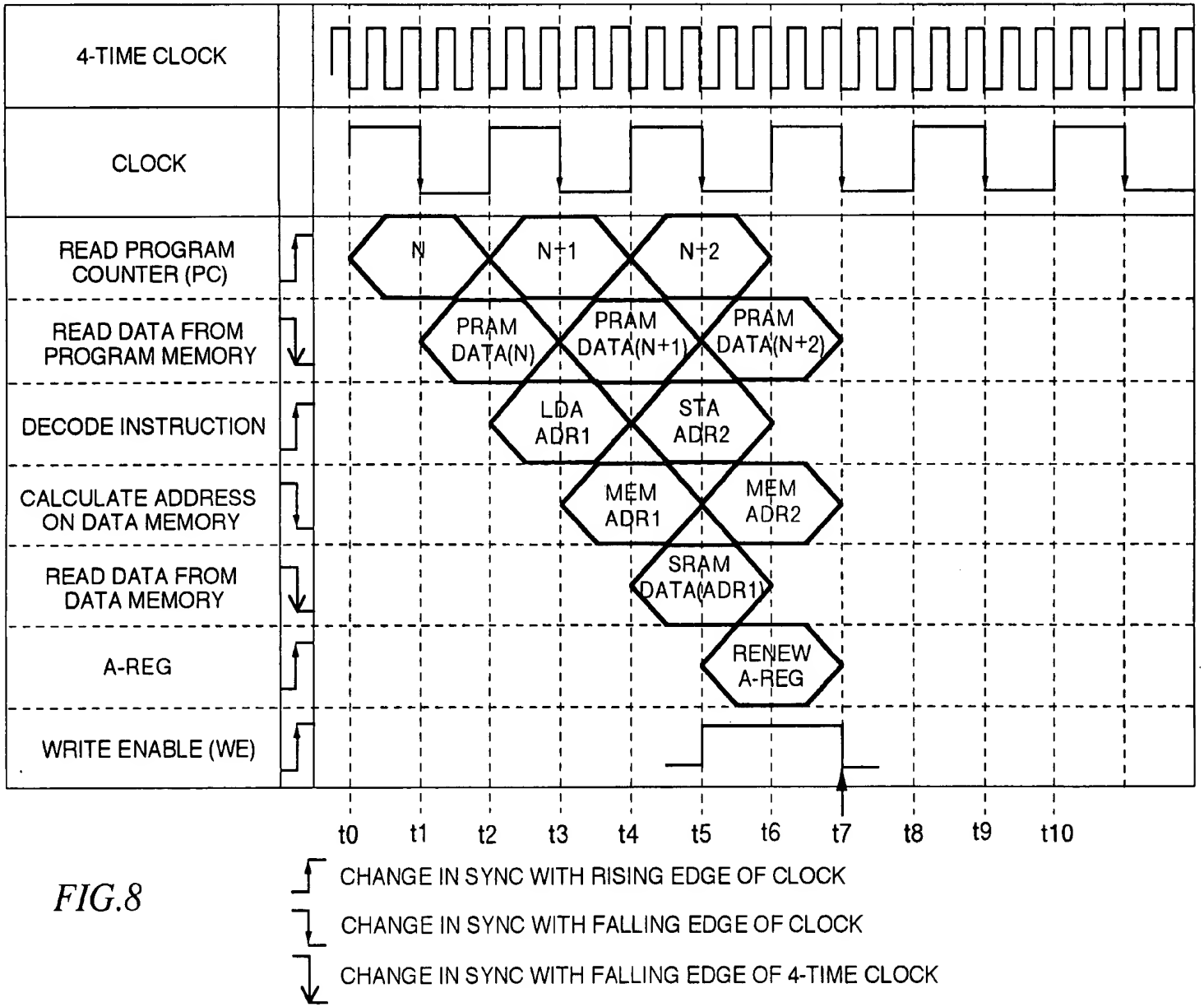


FIG.8

EP 0 712 070 A2 960517

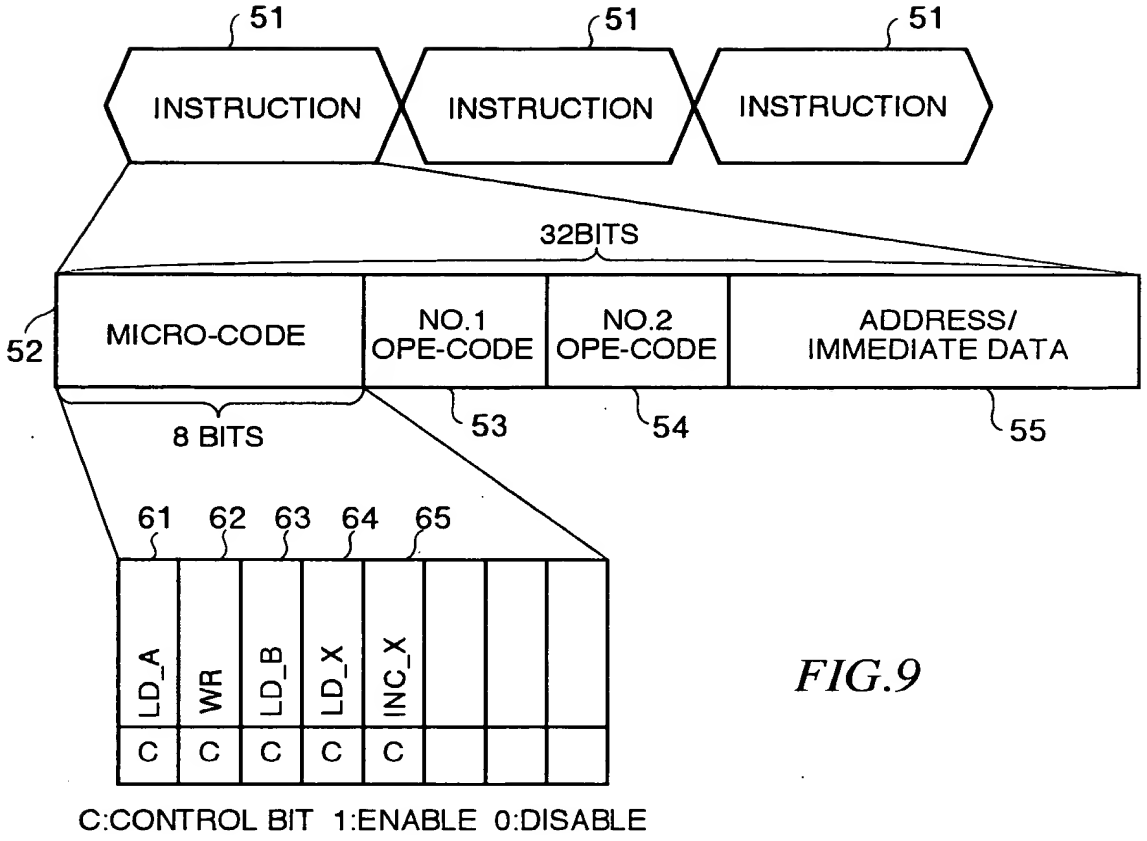
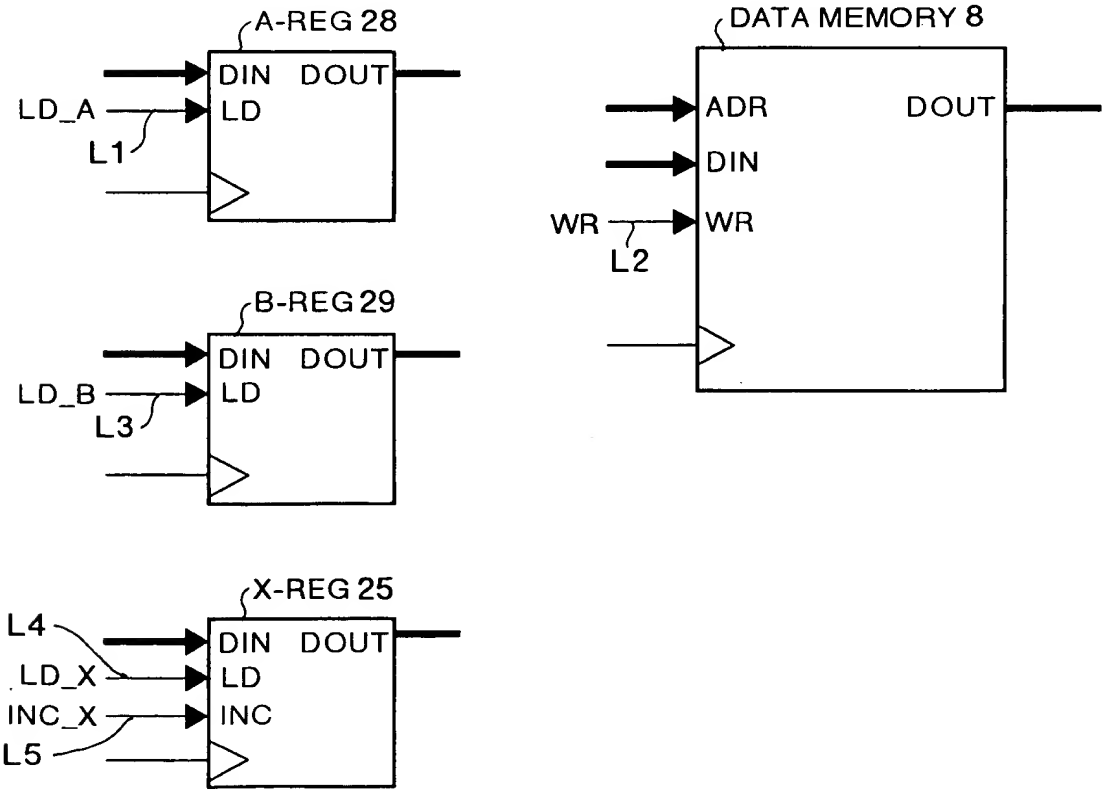


FIG.9



1062170.2002260

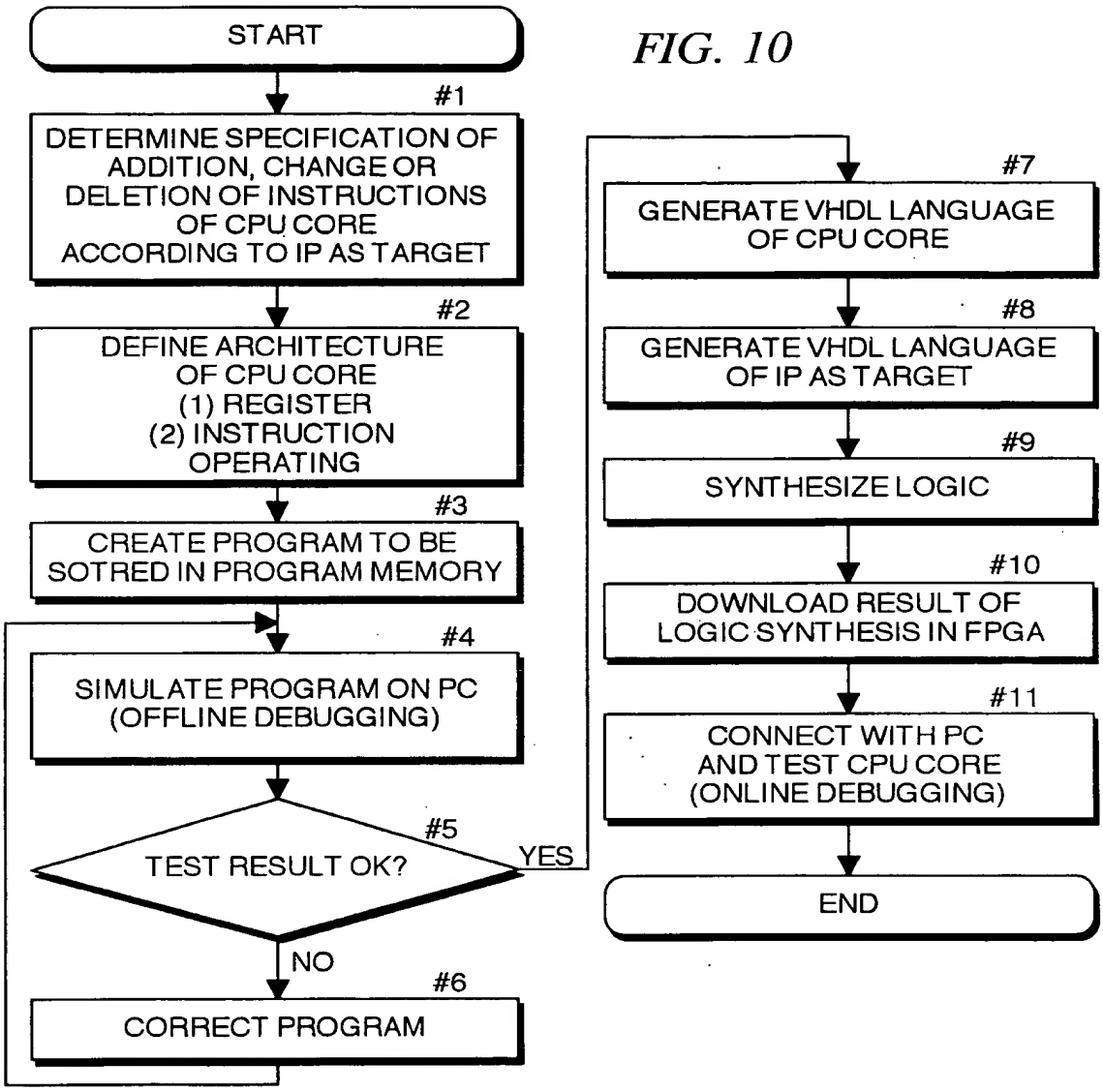


FIG. 10

FIG.11

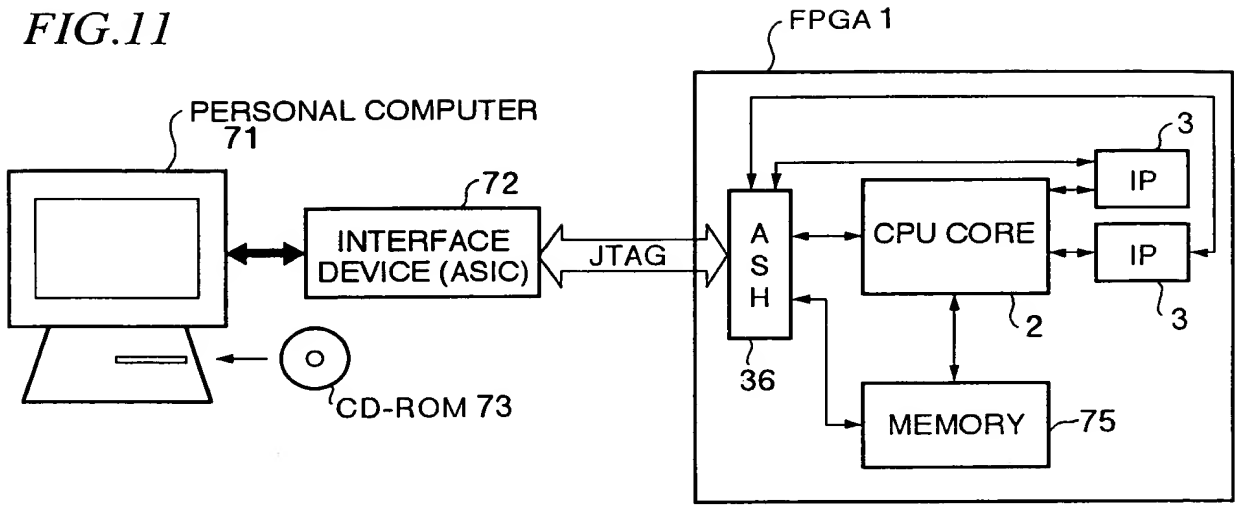
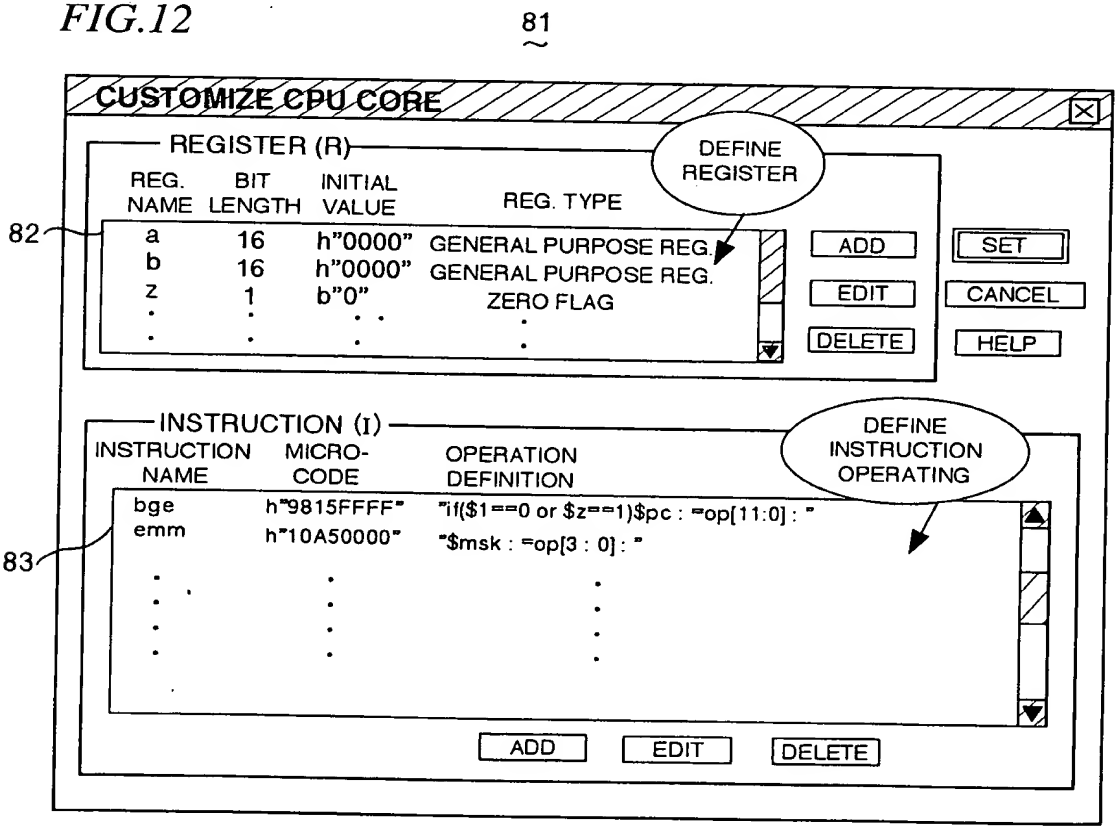

FPGA 1
PERSONAL COMPUTER
71
72
INTERFACE DEVICE (ASIC)
JTAG
A S H
36
CPU CORE
2
IP
3
IP
3
MEMORY
75
CD-ROM 73

FIG.12


81
CUSTOMIZE CPU CORE
REGISTER (R)
DEFINE REGISTER
REG. NAME
BIT LENGTH
INITIAL VALUE
REG. TYPE
82
a 16 h"0000" GENERAL PURPOSE REG.
b 16 h"0000" GENERAL PURPOSE REG.
z 1 b"0" ZERO FLAG
ADD
EDIT
DELETE
SET
CANCEL
HELP
INSTRUCTION (I)
DEFINE INSTRUCTION OPERATING
INSTRUCTION NAME
MICRO-CODE
OPERATION DEFINITION
83
bge h"9815FFFF" "if($1==0 or $z==1)$pc : =op[11:0] : "
emm h"10A50000" "$msk : =op[3 : 0] : "
ADD
EDIT
DELETE